N-Channel Enhancement Mode Power MOSFET

Description

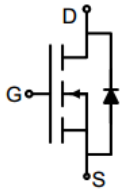
The GT095N10S uses advanced trench technology to provide
excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

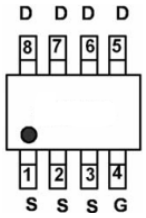
- V_{DS} 100V
- I_D (at V_{GS} = 10V) 21A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 9.5mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 13mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

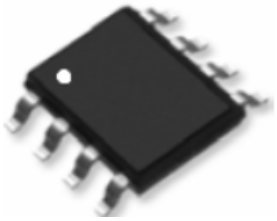
- Synchronous Rectification in SMPS or LED Driver
- UPS
- Motor Control
- BMS
- High Frequency Circuit



Schematic diagram



Marking and pin assignment


SOP-8

Device	Package	Marking	Packaging
GT095N10S	SOP-8	GT095N10	4000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current	I_D	21	A
Pulsed Drain Current (note1)	I_{DM}	85	A
Gate-Source Voltage	V_{GS}	±20	V
Power Dissipation	P_D	8	W
Single pulse avalanche energy （note3）	E_{AS}	60	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	ºC

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	16	ºC/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	75	ºC/W

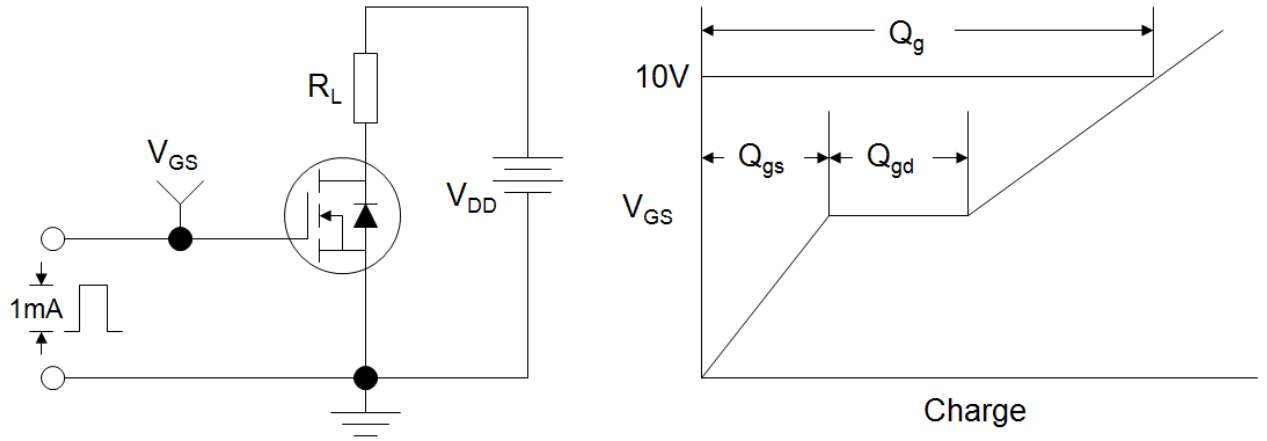
Specifications T_J = 25ºC, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	2	2.6	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	--	8.2	9.5	mΩ
		V_{GS} = 4.5V, I_D = 10A	--	11.3	13	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=20A	--	15.5	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1.0MHz	--	2131	--	pF
Output Capacitance	C_{oss}		--	606	--	
Reverse Transfer Capacitance	C_{rss}		--	21	--	
Total Gate Charge	Q_g	V_{DD} = 50V, I_D = 20A, V_{GS} = 10V	--	29.4	--	nC
Gate-Source Charge	Q_{gs}		--	9	--	
Gate-Drain Charge	Q_{gd}		--	5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 50V, I_D = 20A, R_G = 3Ω	--	17	--	ns
Turn-on Rise Time	t_r		--	4	--	
Turn-off Delay Time	$t_{d(off)}$		--	32	--	
Turn-off Fall Time	t_f		--	8	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	21	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_S= 20A, V_{GS} = 0V	--	--	1.0	V

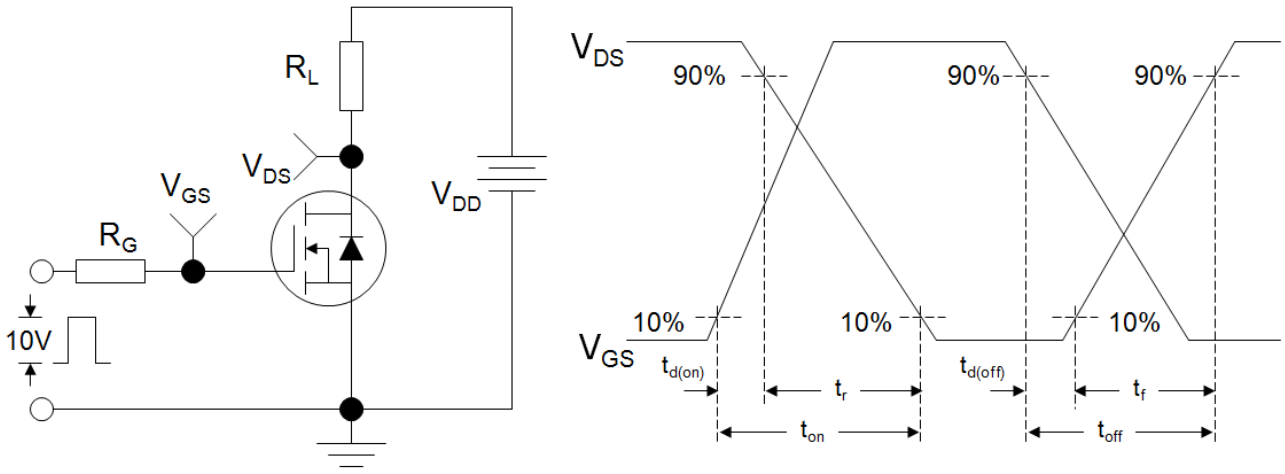
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G
3. EAS condition : Tj=25 ,VDD=50V,VG=10V,L=0.5mH,Rg=25Ω

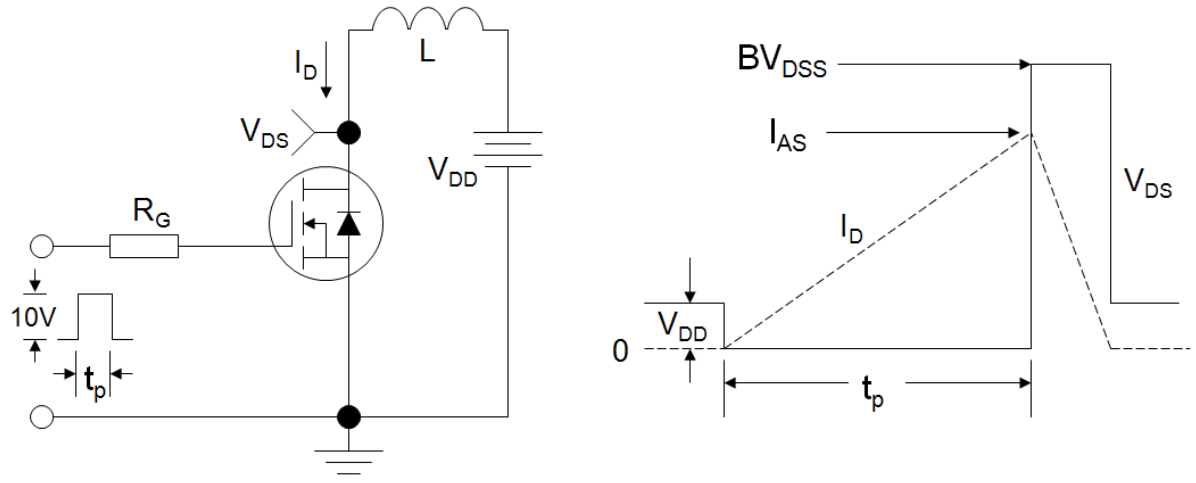
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

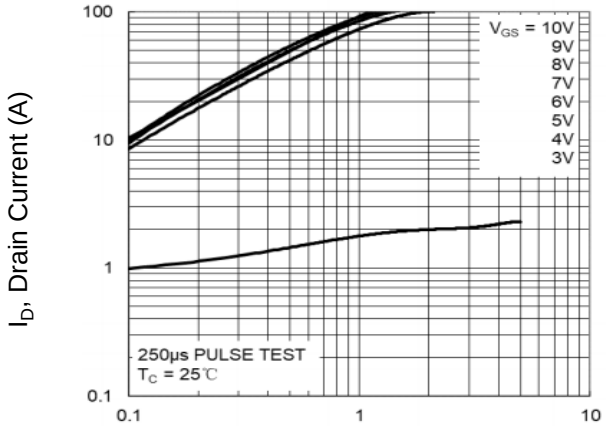


Figure 2. Transfer Characteristics

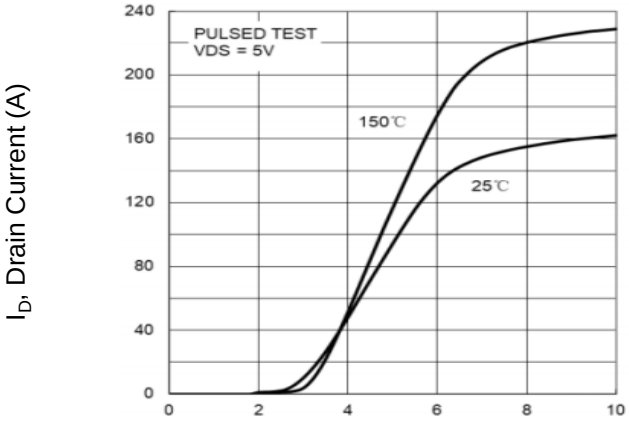


Figure 3. Gate Charge

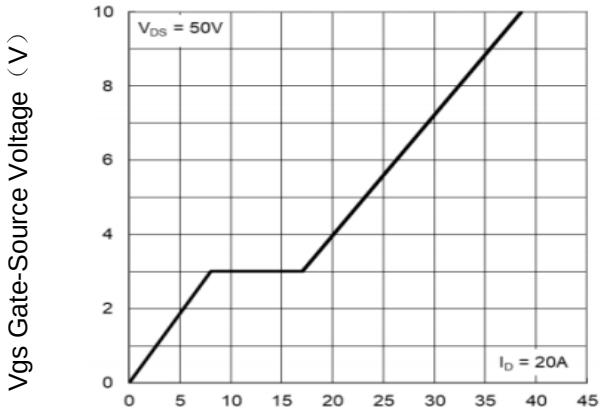


Figure 4. Drain Source On Resistance

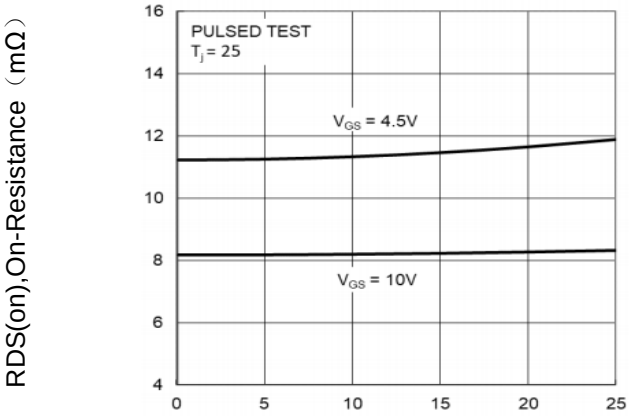


Figure 5. Capacitance

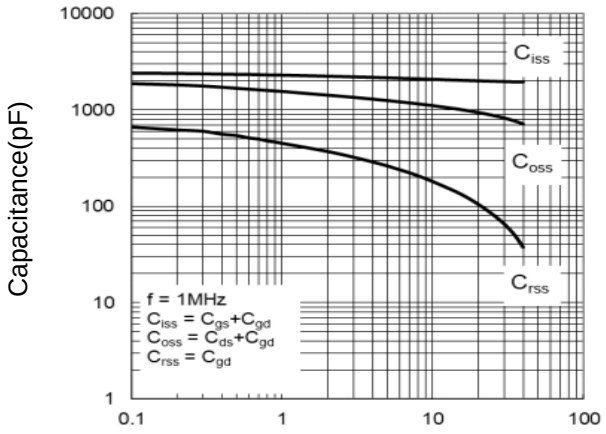
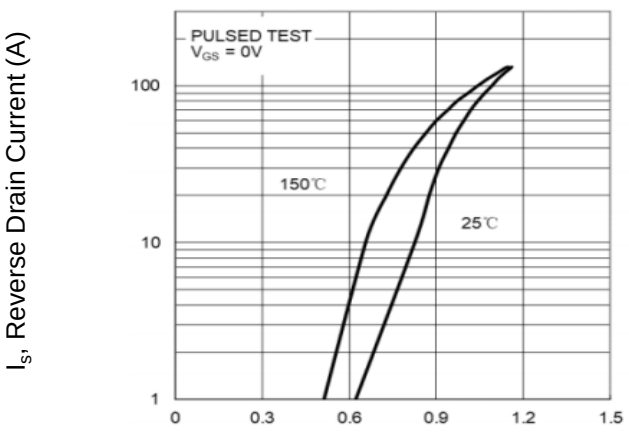


Figure 6. Source-Drain Diode Forward



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

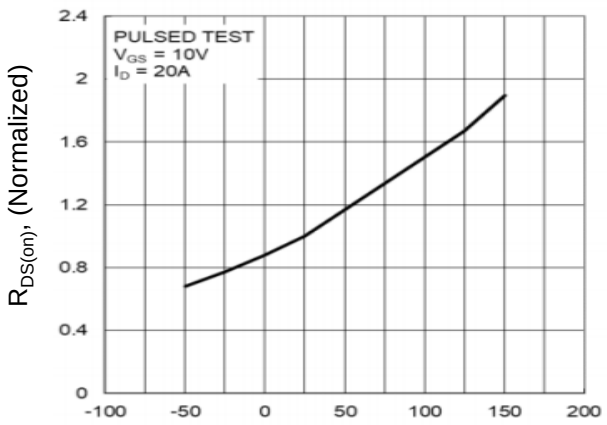


Figure 8. Safe Operation Area

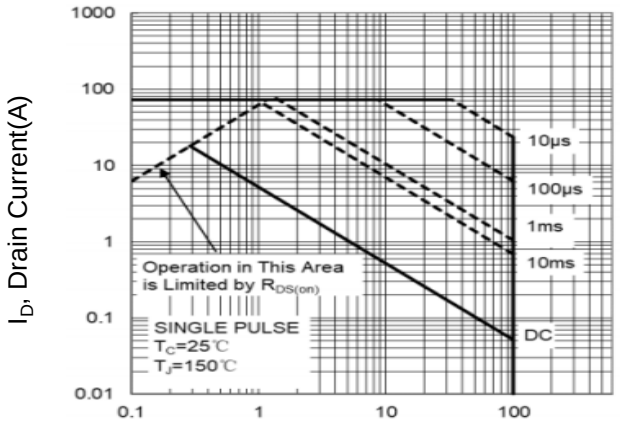
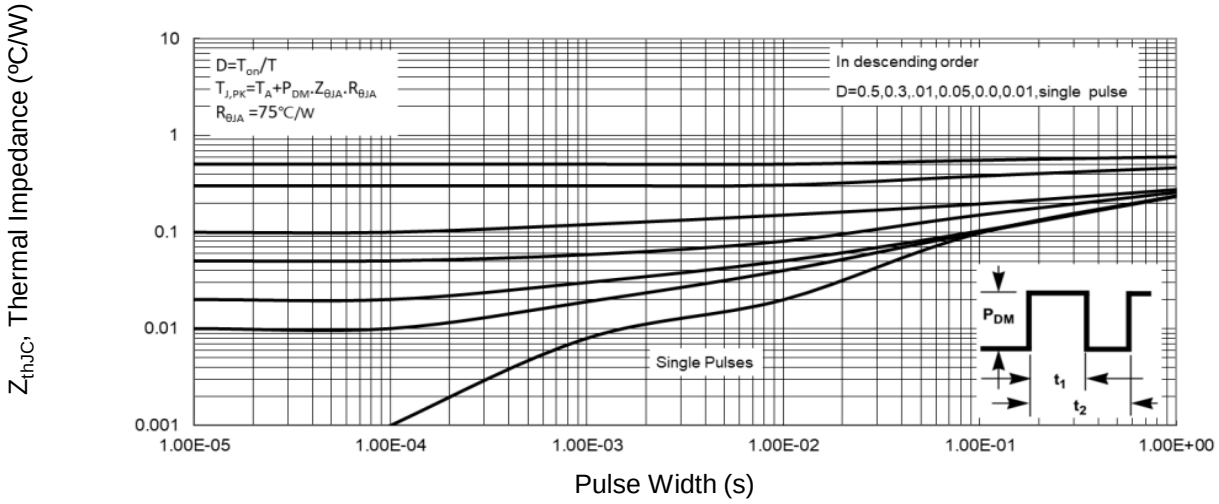
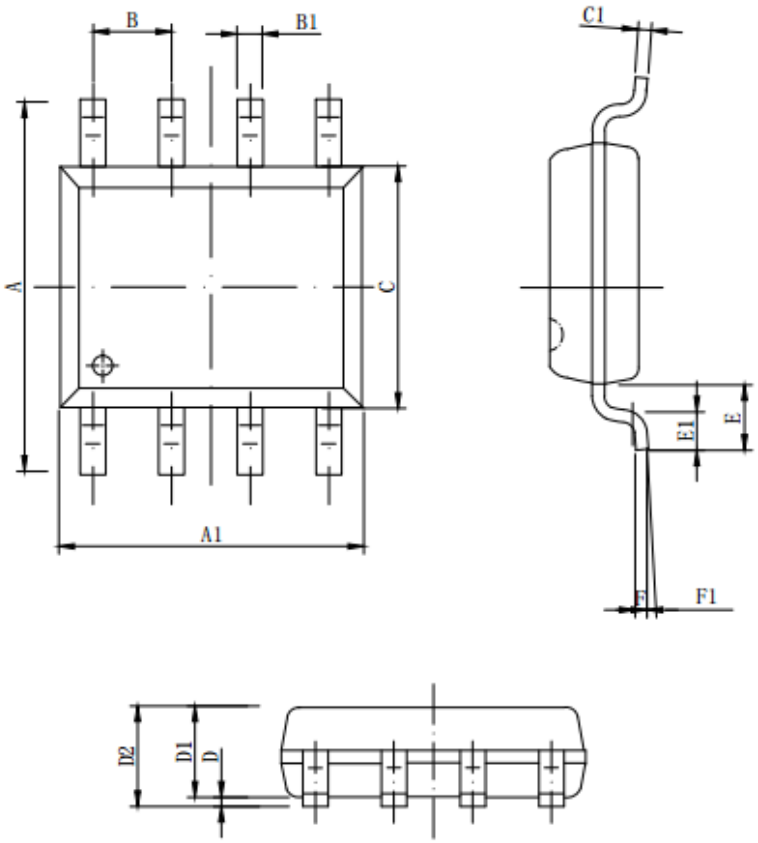


Figure 9. Normalized Maximum Transient Thermal Impedance



SOP-8 Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	5.800	6.000	6.200
A1	4.800	4.900	5.000
B		1.270BSC	
B1	0.35^8x	0.40^8x	0.45^8x
C	3.780	3.880	3.980
C1	--	0.203	0.253
D	0.050	0.150	0.250
D1	1.350	1.450	1.550
D2	1.500	1.600	1.700
D2	1.500	1.600	1.700
E		1.060REF	
E1	0.400	0.700	0.100
F		0.250BSC	
F1	2°	4°	6°